REMARKS

The Office Action dated August 1, 2005 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

The above amendments to claims 1, 3, 14, 15, 16, 20, 25, 26, 27, 31, 35, 37, 40, and 41, and the following remarks, are submitted as a full and complete response thereto.

In accordance with the foregoing, claims 1, 3, 14, 15, 16, 20, 25, 26, 27, 31, 35, 37, 40, and 41 have been amended to improve clarity of the features recited therein and further define the present invention and claim 4 has been cancelled, without prejudice or disclaimer. No new matter is being presented, and approval and entry are respectfully requested. As will be discussed below, it is also requested that all of claims 1-3, 5-12, 14-23, 25-35, 37-38, and 40-42 be found allowable as reciting patentable subject matter.

Claims 1-3, 5-12, 14-23, 25-35, 37-38, and 40-42 stand rejected and pending and under consideration.

REJECTION UNDER 35 U.S.C. § 112:

In the Office Action, at page 2, claims 40-42 are rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness.

In response, claims 40 and 41 have been amended to improve clarity and antecedent support. Regarding the last recitation of claim 40 which recites, in part, "...based upon an amount of internal memory available for an egress port of the clustered

network switch from which the packet is to be transmitted." It is respectfully indicated that the term "from" does not mean that the packet originated from the clustered network. Instead, based upon the amount of internal memory available, the egress port of the clustered network switch would transmit the packet. The first recitation of the claim recites, "receiving a packet in a clustered network switch." It is clear that the packet is received in the clustered network switch and transmitted via an egress port of the clustered network switch. Thus, it is respectfully requested that the § 112, second paragraph rejection of this portion of the claim be withdrawn.

Accordingly, it is respectfully requested that the § 112, second paragraph rejections to the claims be withdrawn. Claims 40-42 are solely rejected under 35 USC § 112, second paragraph. Thus, because claims 40-42 have been amended to improve clarity and antecedent support, and thereby in compliance with 35 U.S.C. § 112, second paragraph, it is respectfully asserted that claims 40-42 are now in condition for allowance.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 1-4, 6-10, 12, 14-22, 25-33, 35, and 37-38 were rejected under 35 U.S.C. § 102 as being anticipated by U. S. Patent No. 6,246,680 to Muller et al. ("Muller"). The Office Action took the position that Muller describes all the recitations of independent claims 1, 14, 15, 16, 20, 25, 26, 27, 31, 35, and 37and

related dependent claims. It is respectfully asserted that, for at least the reasons provided herein below, Muller fails to teach or suggest the recitations of the pending claims. Reconsideration is requested.

Independent claim 1, upon which claims 2, 3, and 5-12 are dependent, recites a network switch, the network switch comprising at least one data port interface supporting a plurality of data ports, at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit data between the network switch and other network switches to create a full duplex configuration, and a CPU interface, the CPU interface configured to communicate with a CPU. A memory management unit is in communication with the at least one data port interface and the at least one stack link interface, and a memory interface is in communication with the at least one data port interface and the at least one stack link interface, wherein the memory interface is configured to communicate with a memory. A communication channel is provided for communicating data and messaging information between the at least one data port interface, the at least one stack link interface, the memory interface, and the memory management unit. The memory management unit is configured to route data received from each of the at least one data port interface and the at least one stack link interface to the memory interface.

Independent claim 14, upon which claims 21-23 are dependent, recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the

predetermined number of switch building blocks comprises at least one data port interface supporting a plurality of data ports for transmitting and receiving data, a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration, and a CPU interface configured to communicate with a CPU. A memory management unit is in communication with the at least one data port interface and the predetermined number of stack link interfaces, a memory interface is in communication with the at least one data port interface and the predetermined number of stack link interfaces, wherein the memory interface is configured to communicate with a memory, and a communication channel is provided for communicating data and messaging information between the at least one data port interface, the predetermined number of stack link interfaces, the memory interface, and the memory management unit.

Claim 15 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch buildings blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex

configuration. Also, the predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 16 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration. Also, the at least one data port interface includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 20 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the

predetermined number of building blocks to create a full duplex configuration, wherein each of the predetermined number of stack link interfaces further comprise a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another switch building block.

Claim 25 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises: at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration. At least one of the predetermined number of switch building blocks further comprises: a CPU interface configured to communicate with a CPU, a memory management unit in communication with the at least one data port interface and the predetermined number of stack link interfaces, a memory interface in communication with the at least one data port interface and the predetermined number of stack link interfaces, wherein the memory interface is configured to communicate with a memory, and a communication channel, the communication channel for communicating data and messaging information between the at least one data port interface, the predetermined number of stack link interfaces, the memory interface, and the memory management unit.

Claim 26 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises: at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration, wherein the predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 27 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises: at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration. The at least one data port interface further comprises: at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate,

and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 31 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises: at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration, wherein each of the predetermined number of stack link interfaces further comprise a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another building block.

Claim 35 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks comprises: at least one data port interface supporting a plurality of data ports for transmitting and receiving data, and a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks to create a full duplex configuration, the

scalable network switch further comprising a physical layer transceiver in connection with at least one of the plurality of data ports.

Claim 37 recites a method of stacking network switches. The method includes providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks, wherein the step of providing a plurality of clustered switch blocks further comprises the steps of: providing a predetermined number of switch building blocks, and interconnecting each of the predetermined number of switch building blocks to every other one of the predetermined number of switch building blocks in a meshed configuration. Each of the predetermined number of switch building blocks is interconnected to every other one of the predetermined number of switch blocks through an individual stack link.

Claim 40 recites a method of stacking network switches, the method comprising the steps of: providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks. The receiving step further comprises the steps of: receiving a packet on at least one of a data port interface and a stack link interface, and storing the packet in a memory in accordance with a predetermined algorithm by allocating memory locations in an internal memory and in an external memory based upon an amount of

internal memory available for an egress port of the clustered network switch from which the packet is to be transmitted.

Claim 41 recites a method of stacking network switches, the method comprising the steps of: providing a plurality of clustered switch blocks, and interconnecting each one of the plurality of clustered switch blocks to another one of the plurality of clustered switch blocks. Interconnection of the plurality of clustered switch blocks forms a stack of clustered switch blocks. The forwarding step further comprises the steps of: determining if the destination address of the packet corresponds to a port in the clustered network switch, forwarding the packet to the port corresponding to the destination address if the destination address is determined to correspond to a port in the clustered network switch, determining if the destination address of the packet corresponds to a port on another clustered network switch across a stack, forwarding the packet to a stack link if the destination address is determined to correspond to a port on the another clustered network switch across the stack, and transmitting the packet across the stack to the another clustered network switch if the destination address of the packet corresponds to a port on the another clustered network switch across the stack.

As will be discussed below, Muller fails to disclose or suggest the elements of any of the presently pending claims.

Muller generally describes an architecture for an integrated network element building block including a network interface 205 with multiple ports for transmitting and receiving packets over a network. See FIG. 2 and column 4, lines 5-67. The network

device building block also includes a packet buffer storage which is coupled to the network interface. The packet buffer storage acts as an elasticity buffer for adapting between incoming and outgoing bandwidth requirements. A shared memory manager 220 is provided to allocate and deallocate buffers in the packet buffer storage on behalf of the network interface and other clients of the packet buffer storage. The network device 205 building block further includes a switch fabric 210 which is coupled to the network interface 205. The switch fabric 210 provides forwarding decisions for received packets. A given forwarding decision includes a list of ports upon which a particular received packet is to be forwarded. A central processing unit (CPU) interface 215 is also included in the network device building block. The CPU interface 215 is coupled to the switch fabric 210 and is configured to forward packets received from the CPU based upon forwarding decisions provided by the switch fabric 210.

Muller provides that a number of external ports (not shown) having input and output capability interface the external connections 117 are provided. Each subsystem supports multiple Gigabit Ethernet ports, Fast Ethernet ports and Ethernet ports. Internal ports (not shown) also having input and output capability in each subsystem couple the internal links 141. Using the internal links, the MLDNE can connect multiple switching elements together to form a multigigabit switch. However, Muller fails to teach or suggest, at least, "at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit data between said network switch and other network switches to create a full duplex configuration," as recited in independent claim 1.

Muller does not teach or suggest in either FIG. 2 or corresponding description that the configuration provided therein is creating a full duplex configuration by including bi-directional gigabit stack link interface to transmit data between network switches. Although Muller provides that the ports have input and output capabilities, that alone does not teach or suggest that the interfaces used in Muller's configuration provides a bi-direction gigabit stack link interface. Also, Muller's configuration does not create a full duplex configuration.

Independent claims 14-16, 20, 25-27, 31, and 35 recite, at least, "a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a full duplex configuration." Because independent claims 14-16, 20, 25-27, 31, and 35 include similar claim features as those recited in independent claim 1, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claims 14-16, 20, 25-27, 31, and 35, the arguments presented above supporting the patentability of independent claims 14-16, 20, 25-27, 31, and 35 are incorporated herein to support the patentability of independent claim 1.

Furthermore, the office action indicates that in column 4, lines 10-15, Muller describes, "interconnecting each of said predetermined number of switch building blocks to every other one of said predetermined number of switch building blocks in a meshed configuration, wherein each of said predetermined number of switch building blocks is

interconnected to every other one of said predetermined number of switch blocks through an individual stack link," as recited in part in independent claim 37. However, the referred portion of Muller merely describes that in FIG. 2, Ethernet packets may enter or leave the network switch element 100 through any one of the three interfaces 205, 215, or 225. There is nothing in Muller that describes or illustrates in FIG. 2 a meshed configuration of switch building blocks. There is no description or suggestion in Muller of providing an individual stack link interconnecting every other one of the switch blocks. By simply indicating that three interfaces are provided in which, through one of such interfaces, the Ethernet packets may enter or leave, does not teach or suggest the particular recitations of the configuration recited in independent claim 37.

Accordingly, in view of the foregoing, it is respectfully requested that independent claims 1, 14-16, 20, 25-27, 31, 35, and 37 and related dependent claims be allowed.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 6, claims 5, 23, and 34 were rejected under 35 U.S.C. § 103 as being unpatentable over Muller and U.S. Patent No. 6,775,290 to Merchant et al. ("Merchant"). The Office Action took the position that Muller and Merchant discloses all the aspects of dependent claims 5, 23, and 34. The rejection is traversed and reconsideration is requested.

As will be discussed below, Muller and Merchant fail to disclose or suggest the elements of any of the presently pending claims.

Dependent claim 5 depends from independent claim 1 and recites the additional features of "a variable sized address resolution logic table; and a variable sized VLAN table, wherein said variable sized address resolution logic table and said variable sized VLAN table is in communication with said memory management unit, said at least one stack link interface, and said at least one data port interface." Dependent claim 23 depends from independent claim 14 and recites the additional features of "wherein said external memory is SRAM." Dependent claim 34 depends from independent claim 25 and recites the additional features of "wherein said external memory is SRAM." Because the combination of Muller and Merchant must teach, individually or combined, all the recitations of the base claim and any intervening claims of dependent claims 5, 23, and 34 the arguments presented above supporting the patentability of independent claims 1, 14, and 25 over Muller are incorporated herein.

Merchant generally describes a method to enable a port of a network switch to support connections with multiple VLANs. See column 1, lines 50-55. Each multiport switch 12 includes a media access control (MAC) module 20 that transmits and receives data packets to and from 10/100 Mb/s physical layer (PHY) transceivers 16 via respective reduced media independent interfaces (RMII) 18 according to IEEE 802.3u protocol. Each multiport switch 12 also includes a gigabit MAC 24 for sending and receiving data packets to and from a gigabit PHY 26 for transmission to the gigabit node 22 via a high speed network medium 28. See column 3, lines 38-47.

However, Merchant does not cure the deficiencies of Muller. Similarly to Muller, Merchant fails to teach or suggest, at least, "at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit data between said network switch and other network switches to create a full duplex configuration," as recited in independent claim 1. The configurations illustrated in FIG. 1 and 3A-3C and corresponding descriptions of Merchant and the configuration illustrated in FIG. 2 and corresponding descriptions of Muller do not illustrate a full duplex configuration in which a bi-directional gigabit stack link interface configured to transmit data between network switches. The combination of Muller and Merchant is silent as to teaching all the recitations of independent claim 1.

Independent claims 14 and 25 recite, at least, "a predetermined number of stack link interfaces comprising bi-directional gigabit stack link interfaces configured to transmit data between one of said predetermined number of building blocks and another of said predetermined number of building blocks to create a full duplex configuration." Because independent claims 14 and 25 include similar claim features as those recited in independent claim 1, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claims 14 and 25, the arguments presented above supporting the patentability of independent claims 14 and 25 are incorporated herein to support the patentability of independent claim 1.

Accordingly, in view of the foregoing, it is respectfully requested that independent claims 1, 14, and 25 and related dependent claims 5, 23, and 34, respectively, be allowed.

In the Office Action, at page 6, claim 11 was rejected under 35 U.S.C. § 103 as being unpatentable over Muller and U.S. Patent No. 6,711,171 to Dobbins et al. ("Dobbins"). The Office Action took the position that Muller and Dobbins discloses all the aspects of dependent claim 11. The rejection is traversed and reconsideration is requested.

As will be discussed below, Muller and Dobbins fail to disclose or suggest the elements of any of the presently pending claims.

Dependent claim 11 depends from independent claim 1 and recites the additional features of "wherein said at least one data port interface, said at least one stack link interface, said CPU interface, said memory interface, said memory management unit, and said communication channel are integrated on a single application specific integrated circuit (ASIC) chip." Because the combination of Muller and Merchant must teach, individually or combined, all the recitations of the base claim and any intervening claims of dependent claim 11 the arguments presented above supporting the patentability of independent claim 1 over Muller are incorporated herein.

Dobbins generally describes a topology services including a link state topology exchange among switches, which provides each switch with a complete topology graph of the network. This enables an access switch receiving a data packet to determine a complete path from a source end system to a destination end system. Another service includes resolution of broadcast frames to unicast frames, in order to reduce the amount of broadcast traffic. Policy restrictions may be applied prior to connection setup. Path

determination services enable multiple paths from a source to a destination. Connection management includes source routed mapping of connections on the desired path. A distributed call rerouting service is provided wherein if a link on an active path fails, each switch receives a topology change notification and unmaps any connection involving the failed link.

However, Dobbins does not cure the deficiencies of Muller. Similarly to Muller, Dobbins fails to teach or suggest, at least, "at least one stack link interface comprising a bi-directional gigabit stack link interface configured to transmit data between said network switch and other network switches to create a full duplex configuration," as recited in independent claim 1. The configuration described in Dobbins is different from a full duplex configuration and there is no teaching or suggestion of a bi-directional gigabit stack link interface used in the topology described in Dobbins. The configuration illustrated in FIG. 1, 15, and 20 and corresponding descriptions of Dobbins and the configuration illustrated in FIG. 2 and corresponding descriptions of Muller do not illustrate a full duplex configuration in which a bi-directional gigabit stack link interface configured to transmit data between network switches. The combination of Muller and Merchant is silent as to teaching all the recitations of independent claim 1.

Accordingly, in view of the foregoing, it is respectfully requested that independent claim 1 and related dependent claim 11 be allowed.

CONCLUSION:

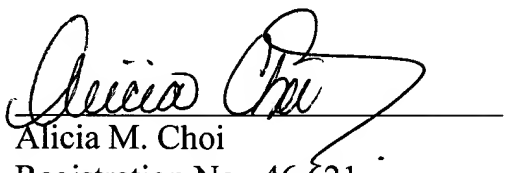
In view of the above, Applicant respectfully submits that the claimed invention recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant further submits that the subject matter is more than sufficient to render the claimed invention unobvious to a person of skill in the art. Applicant therefore respectfully requests that each of claims 1-3, 5-12, 14-23, 25-35, 37-38, and 40-42 be found allowable and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Alicia M. Choi
Registration No. 46,621

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

AMC:kmp